forming a p transistor and an n transistor in the heterostructure, wherein the strained layer comprises a channel of at least one of the transistors, the transistors being interconnected in a CMOS circuit.

6 ~~33.~~ The method of claim ~~32~~ 5 wherein the heterostructure further comprises an insulating layer below the strained layer.

7 ~~34.~~ The method of claim ~~32~~ 15 ~~32~~ 5 wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

8 ~~35.~~ The method of claim ~~32~~ 5 wherein the strained layer comprises Si.

9 ~~36.~~ The method of claim ~~32~~ 5 wherein $0.1 < x < 0.5$.

10 ~~37.~~ The method of claim ~~32~~ 5 wherein the CMOS circuit comprises a logic gate.

11 ~~38.~~ The method of claim ~~37~~ 10 wherein the logic gate is a NOR gate.